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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10077258	02/14/2002	257	324	2814	

**APPLICANTS: Mo Brian; Chau Duc; *W*

**CONTINUING DATA VERIFIED: *yes*

THIS APPLICATION IS A DIV OF 09/286,168 04/05/1999 *W*

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** FOREIGN APPLICATIONS VERIFIED: *None* *W*

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed		<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	
35 USC 119 conditions met		<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	018865-001010US
Verified and Acknowledged Examiner's initials <i>W</i>			
TITLE : Method of forming a trench transistor having a superior gate dielectric			
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L(Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		<i>Yenn Lu B. Hwang</i> Assistant Examiner	
ISSUE FEE		Primary Examiner	
Amount Due	Date Paid	Total Claims 10	Print Claim for O.G 1
TERMINAL		DRAWING	
DISCLAIMER		Sheets Drwg. 5	Figs.Drwg. 7
		Print Fig. 3,4	
PREPARED FOR ISSUE		Application Examiner	
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